AD - Converter

ADC0804

8-Bit AD – Converter

DATASHEET

OEM – Intersil

Source: Intersil Databook 1987

Datasheet Rev. 1.0 – 10/20 – data without warranty / liability

ADC0802 - ADC0804
8-Bit μP-Compatible A/D Converters

GENERAL DESCRIPTION

The ADC0802 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

FEATURES

- **80C48 and 80C80/85 Bus Compatible — No Interfacing Logic Required**
- **Conversion Time < 100μs**
- **Easy Interface to Most Microprocessors**
- **Will Operate in a "Stand Alone" Mode**
- **Differential Analog Voltage Inputs**
- **Works With Bandgap Voltage References**
- **TTL Compatible Inputs and Outputs**
- **On-Chip Clock Generator**
- **0V to 5V Analog Voltage Input Range (Single +5V Supply)**
- **No Zero-Adjust Required**

ORDERING INFORMATION

Part Number	Error	Temperature Range	Package
ADC0802LCN	±½ bit no adjust	0°C to +70°C	20 pin Plastic DIP
ADC0802LCD	±¾ bit no adjust	−40°C to +85°C	20 pin CERDIP
ADC0802LD	±1 bit no adjust	−55°C to +125°C	20 pin CERDIP
ADC0803LCN	±½ bit adjusted full-scale	0°C to +70°C	20 pin Plastic DIP
ADC0803LCD	±¾ bit adjusted full-scale	−40°C to +85°C	20 pin CERDIP
ADC0803LD	±1 bit adjusted full-scale	−55°C to +125°C	20 pin CERDIP
ADC0804LCN	±1 bit no adjust	0°C to +70°C	20 pin Plastic DIP
ADC0804LCD	±1 bit no adjust	−40°C to +85°C	20 pin CERDIP

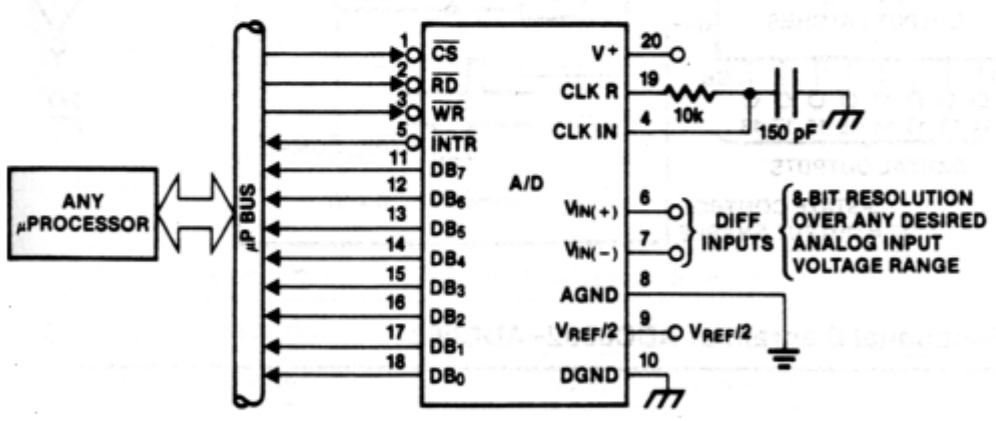

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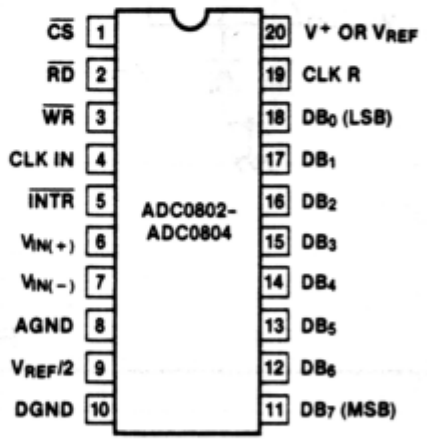
Figure 1: Typical Application



TOP VIEW

0334-2

(Outline dwg. CD, CN)

Figure 2: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

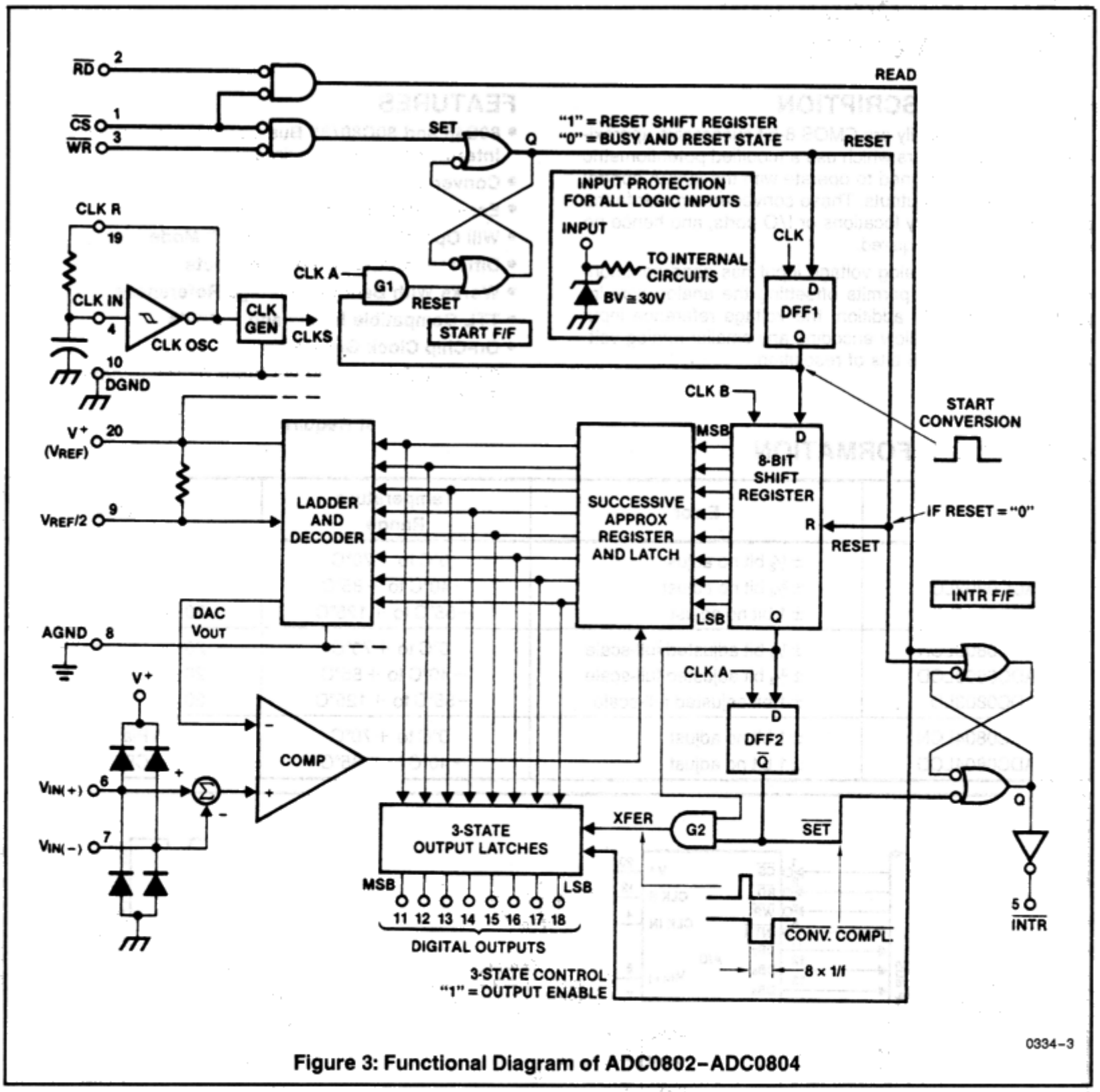


Figure 3: Functional Diagram of ADC0802-ADC0804

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Voltage at Any Input ..... −0.3V to (V+ +0.3V)
Storage Temperature Range ..... −65°C to +150°C
Package Dissipation at T_A = +25°C 875mW
Lead Temperature (Soldering, 10sec) ..... 300°C

OPERATING RATINGS

Temperature Range
ADC0802/03LD ..... −55°C to +125°C
ADC0802/03/04LCD ..... −40°C to +85°C
ADC0802/03/04LCN ..... 0°C to +70°C
Supply Voltage Range ..... 4.5V to 6.3V

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Notes 1 and 7)

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $T_A = +25°C$ and $f_{CLK} = 640kHz$ unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	Completely Unadjusted			±½	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±½	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND−0.05		V^+ +0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	$V^+ = 5V$ ±10% Over Allowed Input Voltage Range		± 1/16	± ⅛	LSB

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $0°C \le T_A \le +70°C$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	Completely Unadjusted			±½	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±½	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND−0.05		V^+ +0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	$V^+ = 5V$ ±10% Over Allowed Input Voltage Range		± 1/16	± ¼	LSB

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

INTERSIL

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $-25°C \leq T_A \leq +85°C$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	Completely Unadjusted			±¾	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±¾	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND−0.05		$V^+ + 0.05$	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±⅛	±¼	LSB
Power Supply Sensitivity	$V^+ = 5V$ ±10% Over Allowed Input Voltage Range		±1/16	±⅛	LSB

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $-55°C \leq T_A \leq +125°C$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	Completely Unadjusted			±1	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±1	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			±1¼	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND−0.05		$V^+ + 0.05$	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±⅛	±¼	LSB
Power Supply Sensitivity	$V^+ = 5V$ ±10% Over Allowed Input Voltage Range		±⅛	±¼	LSB

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

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DC ELECTRICAL CHARACTERISTICS
Digital Levels and DC Specifications: $V^+ = 5V$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CONTROL INPUTS (Note 6)						
V_{INH}	Logical "1" Input Voltage (Except Pin 4 CLK IN)	$V^+ = 5.25V$	2.0		V^+	V
V_{INL}	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V^+ = 4.75V$			0.8	V
V^+_{CLK}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V
V^-_{CLK}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V
V_H	CLK IN (Pin 4) Hysteresis $(V_{CLK}^+) - (V_{CLK}^-)$		0.6	1.3	2.0	V
I_{INHI}	Logical "1" Input Current (All Inputs)	$V_{IN} = 5V$		0.005	1	μA
I_{INLO}	Logical "0" Input Current (All Inputs)	$V_{IN} = 0V$	−1	−0.005		μA
I^+	Supply Current (Includes Ladder Current)	$f_{CLK} = 640kHz$, $T_A = +25°C$ and $\overline{CS}$ = HI		1.3	2.5	mA

DC ELECTRICAL CHARACTERISTICS
Digital Levels and DC Specifications: $V^+ = 5V$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted. (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DATA OUTPUTS AND $\overline{INTR}$						
V_{OL}	Logical "0" Output Voltage	$I_o = 1.6mA$ $V^+ = 4.75V$			0.4	V
V_{OH}	Logical "1" Output Voltage	$I_o = -360\mu A$ $V^+ = 4.75V$	2.4			V
I_{LO}	3-State Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−3		3	μA μA
I_{SOURCE}	Output Short Circuit Current	V_{OUT} Short to Gnd $T_A = +25°C$	4.5	6		mA
I_{SINK}	Output Short Circuit Current	V_{OUT} Short to V^+ $T_A = +25°C$	9.0	16		mA

NOTES: 1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.

2. For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see **Block Diagram**) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V^+ supply. Be careful, during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.
3. With $V^+ = 6V$, the digital logic interfaces are no longer TTL compatible.
4. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.
5. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see **Timing Diagrams**).
6. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.
7. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See **Zero Error** on page 10 of this data sheet.

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

AC ELECTRICAL CHARACTERISTICS

Timing Specifications: $V^+ = 5V$ and $T_A = +25°C$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{CLK}	Clock Frequency	$V^+ = 6V$ (Note 3) $V^+ = 5V$	100 100	640 640	1280 800	kHz kHz
t_{conv}	Clock Periods per Conversion (Note 4)		62		73	
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS} = 0V$, $f_{CLK} = 640kHz$			8888	conv/s
$t_{W(\overline{WR})I}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS} = 0V$ (Note 5)	100			ns
t_{acc}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100pF$ (Use Bus Driver IC for Larger C_L)		135	200	ns
t_{1h}, t_{0h}	3-State Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State)	$C_L = 10pF$, $R_L = 10k$ (See **3-State Test Circuits**)		125	250	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5		pF
C_{OUT}	3-State Output Capacitance (Data Buffers)			5		pF

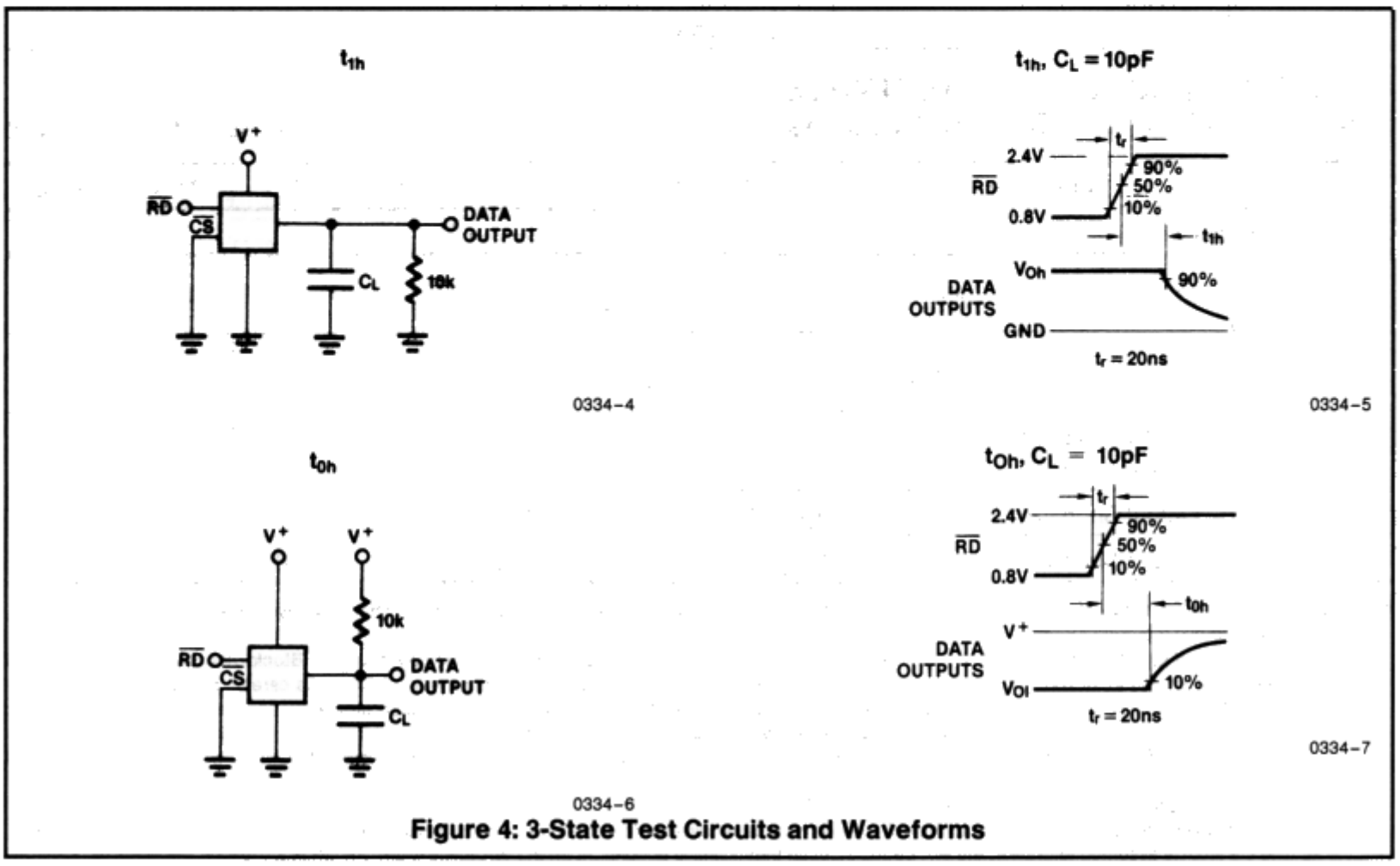


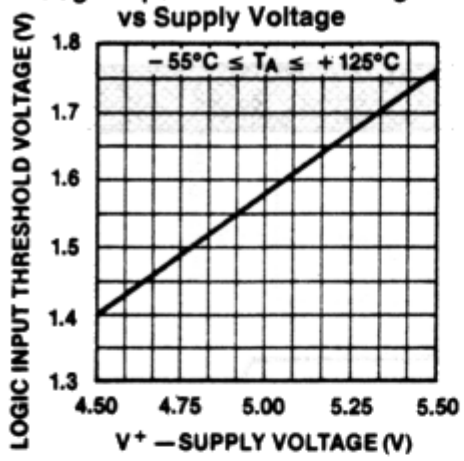
Figure 4: 3-State Test Circuits and Waveforms

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

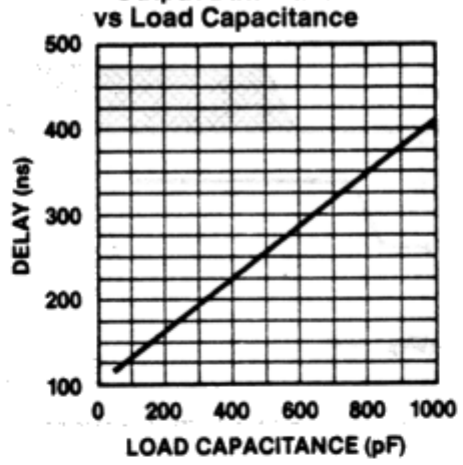
TYPICAL PERFORMANCE CHARACTERISTICS

Logic Input Threshold Voltage vs Supply Voltage



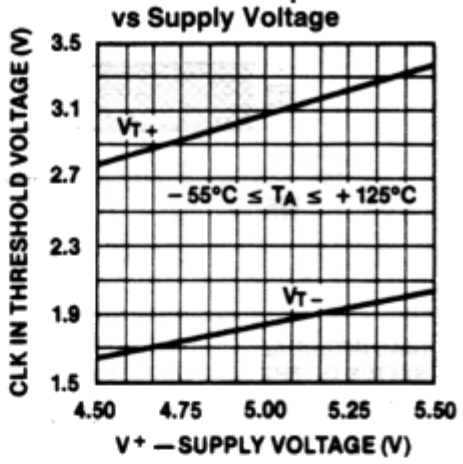
0334-8

Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



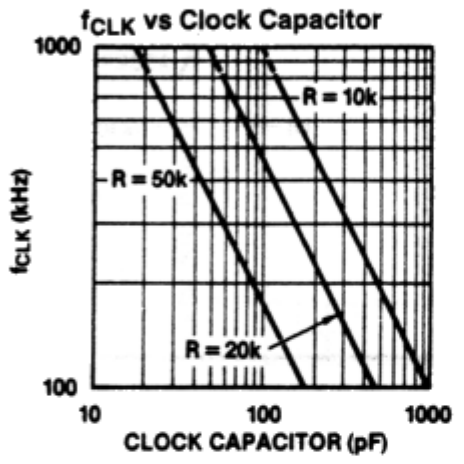
0334-9

CLK IN Schmitt Trip Levels vs Supply Voltage



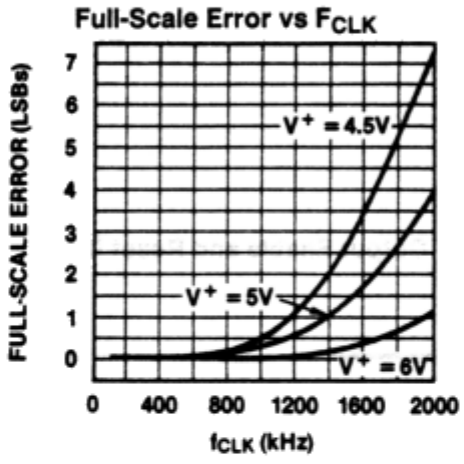
0334-10

f_{CLK} vs Clock Capacitor



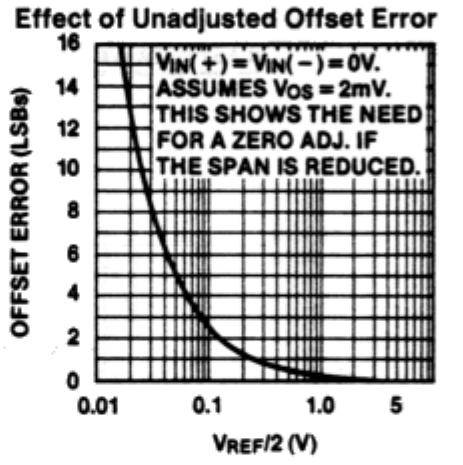
0334-11

Full-Scale Error vs F_{CLK}



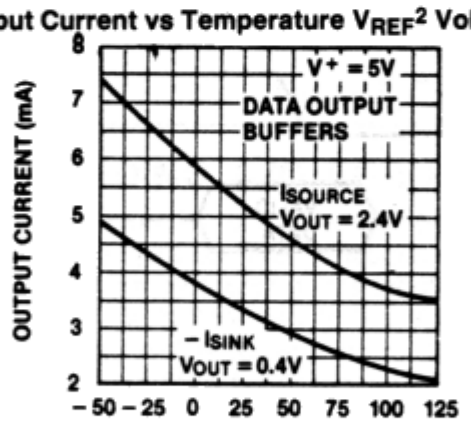
0334-12

Effect of Unadjusted Offset Error



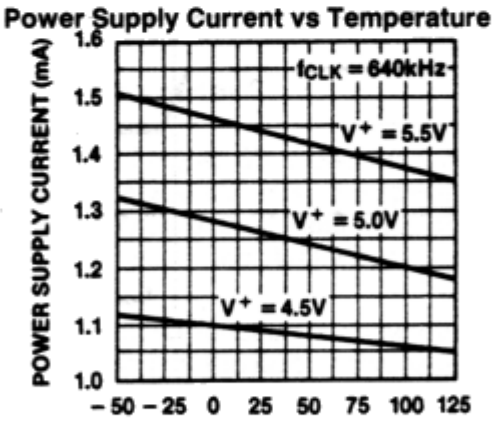
0334-13

Output Current vs Temperature V_{REF}^2 Voltage



0334-14

Power Supply Current vs Temperature



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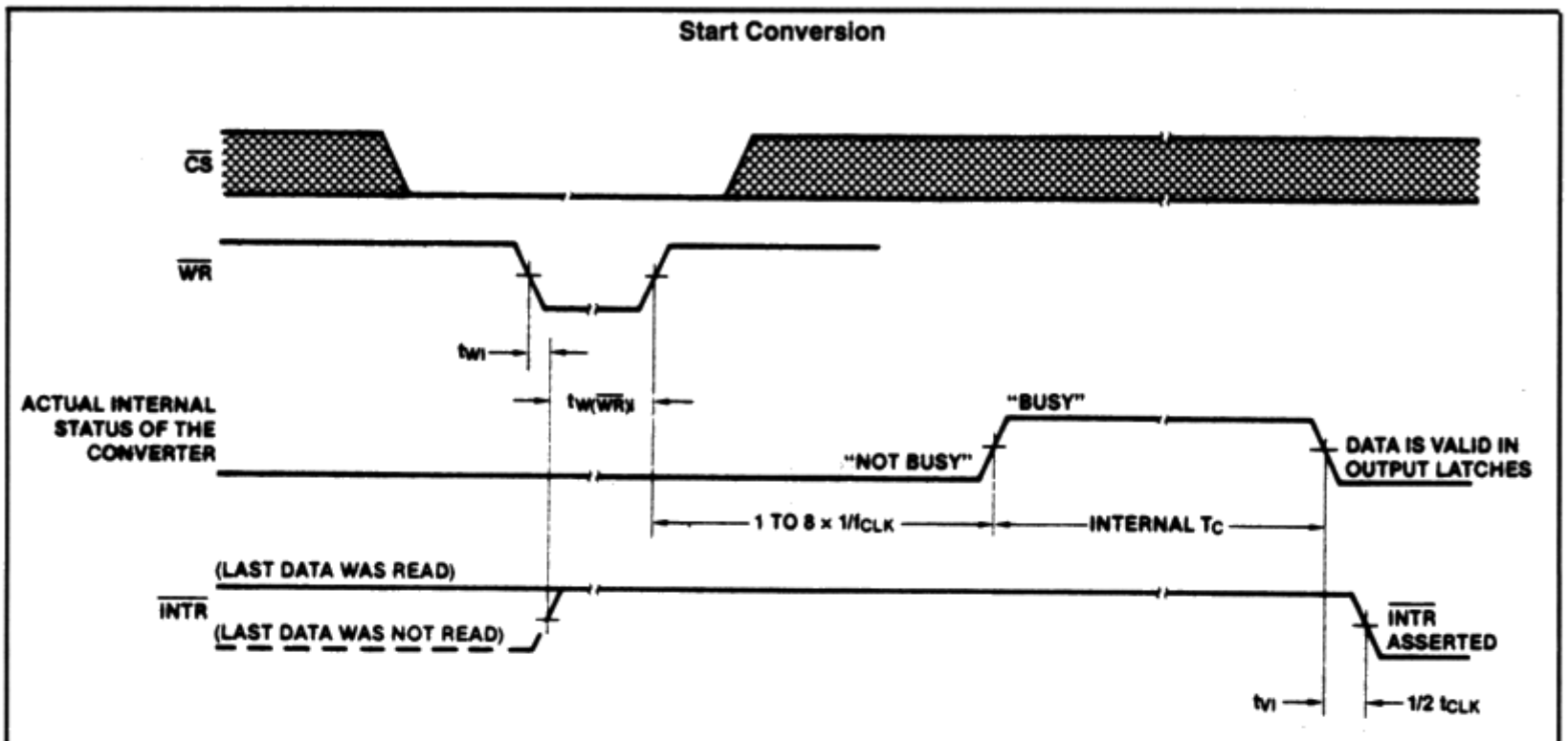
NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

INTERSIL

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



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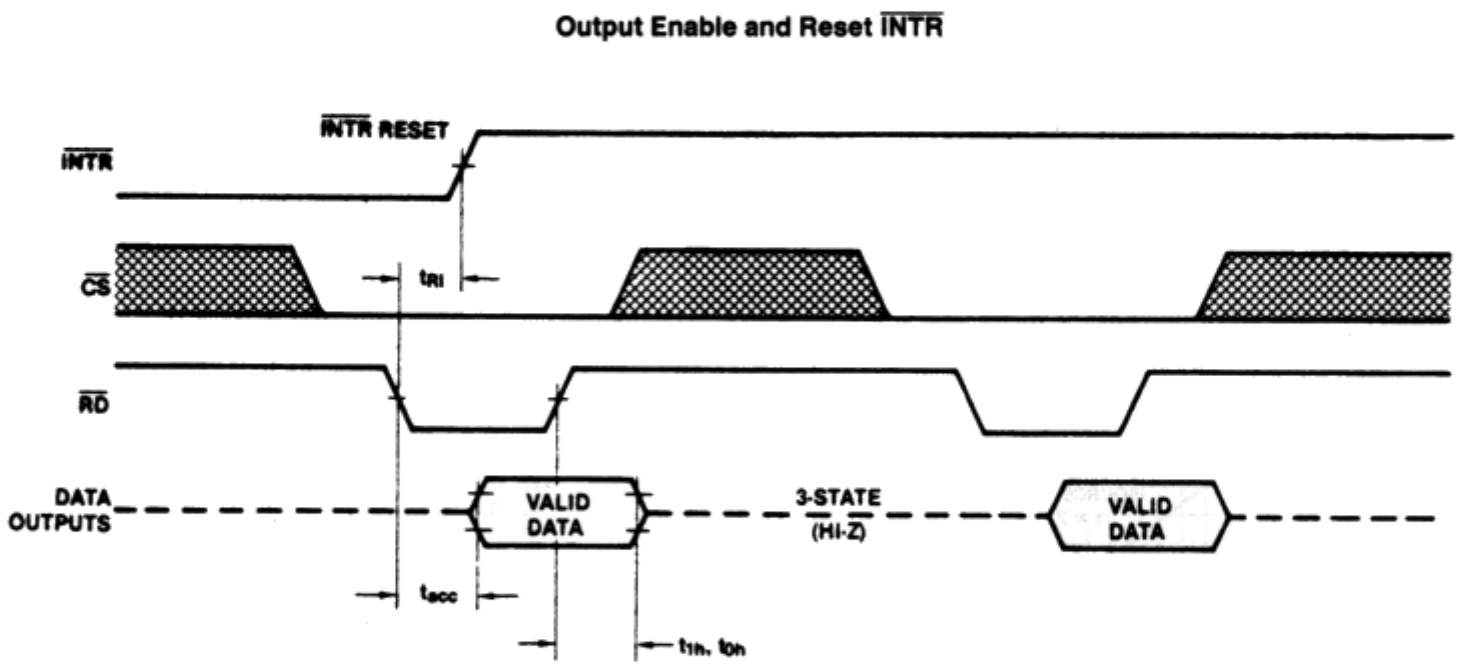


0334-17

0334-17

Figure 5: Timing Diagrams

Note: All timing is measured from the 50% voltage points.

NOTE: All typical values have been characterized but are not tested.

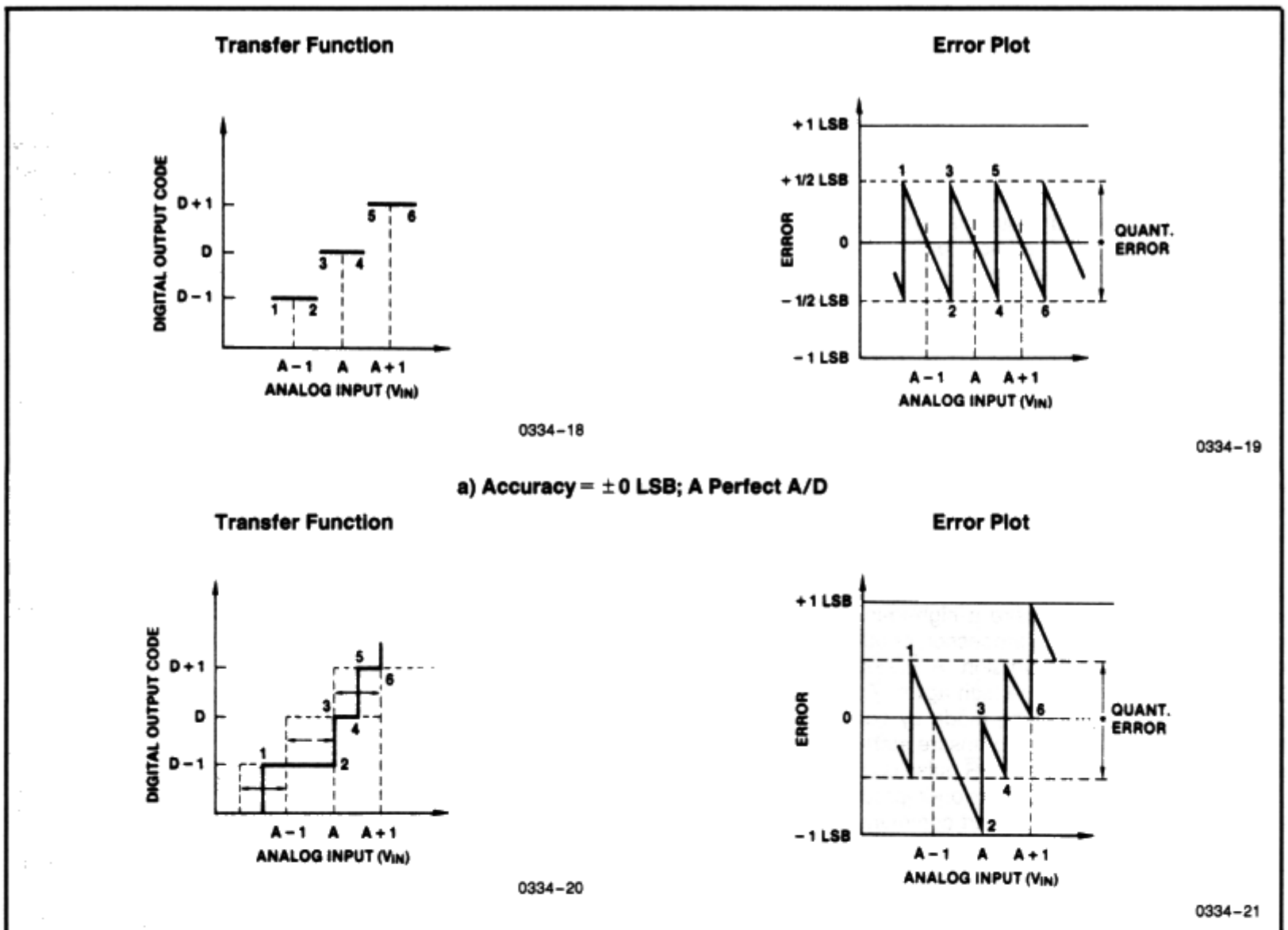


Figure 6: Clarifying the Error Specs of an A/D Converter

UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 6a. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D − 1, D, and D + 1. For the perfect A/D, not only will center-value (A − 1,A,A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1LSB wide.

The error curve of Figure 6b shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 6a is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1LSB in magnitude, unless the device has missing codes.

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

INTERSIL

FUNCTIONAL DESCRIPTION

A functional diagram of the ADC0802 series of A/D converters is shown in Figure 3. All of the package pinouts are shown and the major logic control paths are drawn in heavier-weight lines. The device operates on the successive approximation principle (see APPLICATION NOTE A016 and A020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the $\overline{WR}$ input, the internal SAR latches and the shift-register stages are reset, and the $\overline{INTR}$ output will be set high. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. **Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.** After the requisite number of clock pulses to complete the conversion, the $\overline{INTR}$ pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A $\overline{RD}$ operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line high again. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

Digital Details

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide $\overline{CS}$ and $\overline{WR}$ signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the 3-state output latches. When DFF2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the 3-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard TTL logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the $\overline{WR}$ input (pin 3). The Output Enable function is achieved by an active low pulse at the $\overline{RD}$ input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by ½ LSB (see Figure 6a).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA – 20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_p)(2\pi f_{cm}) \left[\frac{4.5}{f_{CLK}} \right]$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

For example, with a 60Hz common-mode frequency, f_{cm}, and a 640kHz A/D clock, f_{CLK}, keeping this error to ¼ LSB (~5mV) would allow a common-mode voltage, V_P, given by:

$$V_p = \frac{[\Delta V_e(MAX)(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_p = \frac{(5\times10^{-3})\,(640\times10^{3})}{(6.28)\,(60)\,(4.5)} \cong 1.9V$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see **Reference Voltage Span Adjust**).

NOTE: All typical values have been characterized but are not tested.

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and **do not inherently cause errors** as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5μA. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin** for high resistance sources (>1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, **will not cause errors** since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor (≤1kΩ) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications, (≤1kΩ), a 0.1μF bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5kΩ. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capcitors will average the transient input switching currents of the A/D (see **Analog Input Current).** This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full-scale adjustment of the A/D (see **Full-Scale Adjustment)** with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 7.

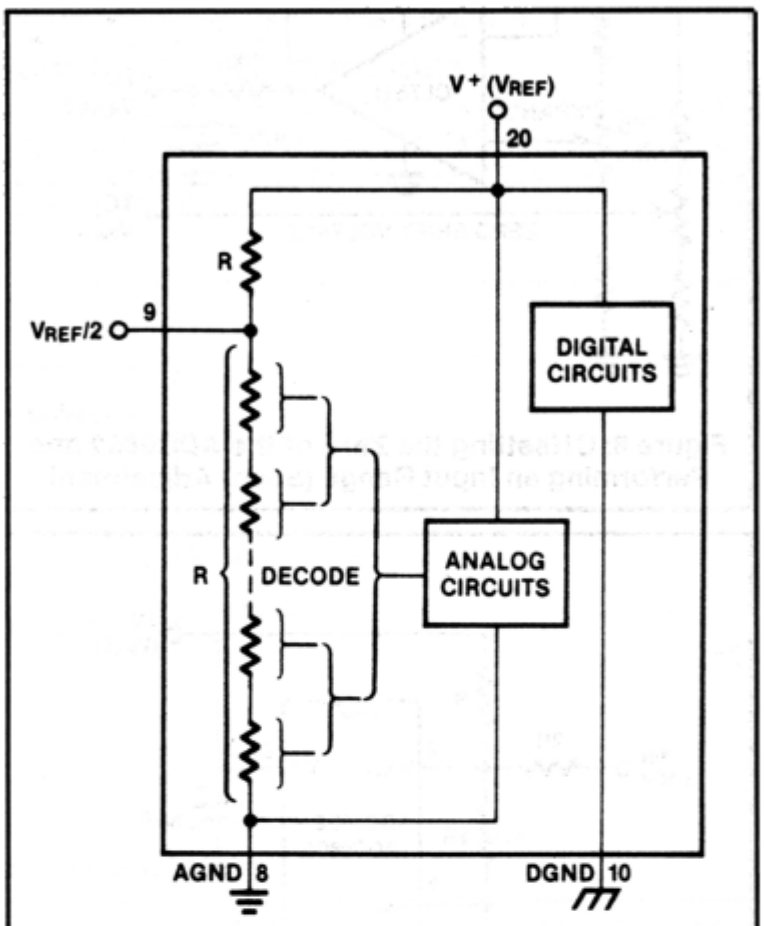


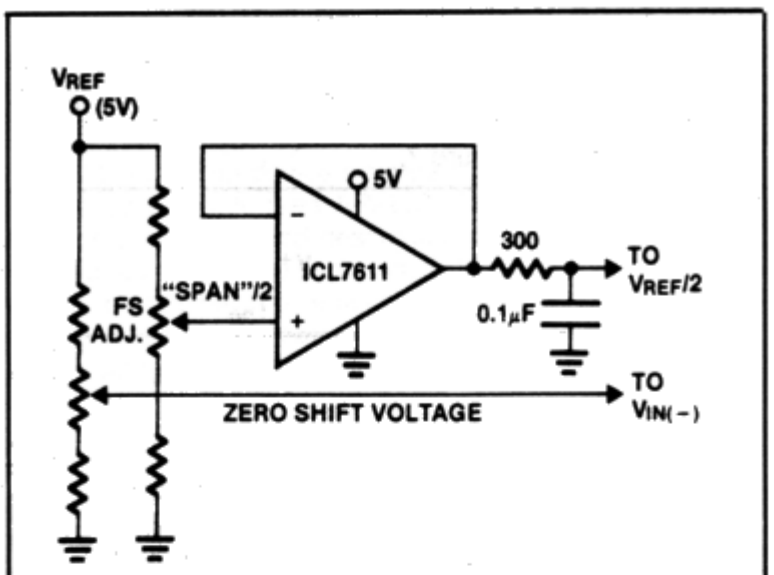
Figure 7: The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage which is applied to the V^+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V^+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 8. For expanded scale inputs, the circuits of Figures 9 and 10 can be used.

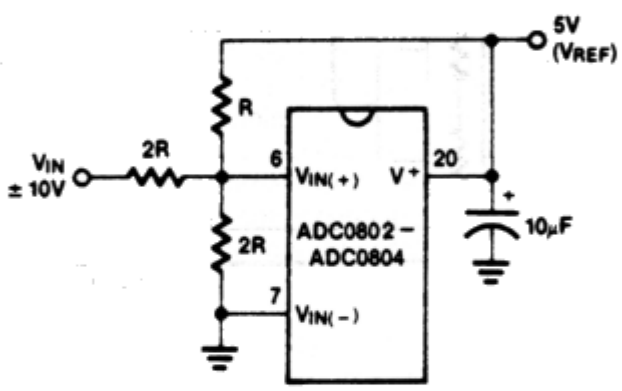
NOTE: All typical values have been characterized but are not tested.

ADC0802–ADC0804



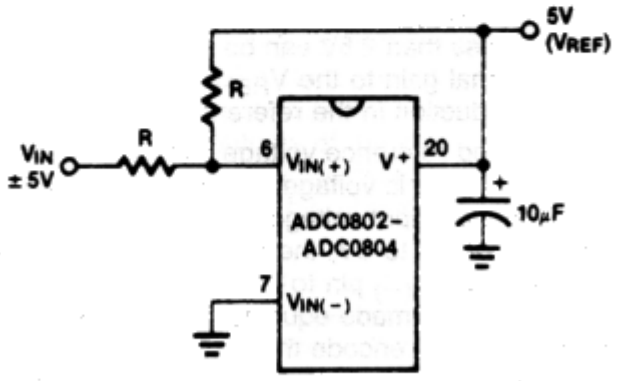
0334–23

Figure 8: Offsetting the Zero of the ADC0802 and Performing an Input Range (Span) Adjustment



0334–24

Figure 9: Handling ± 10V Analog Input Range



0334–25

Figure 10: Handling ± 5V Analog Input Range

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of ±10mV will cause conversion errors of ±1LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see **Applications** section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for $V_{REF}/2 = 2.500V$).

Full-Scale Adjust

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}\text{fsadj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

NOTE: All typical values have been characterized but are not tested.

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 11.

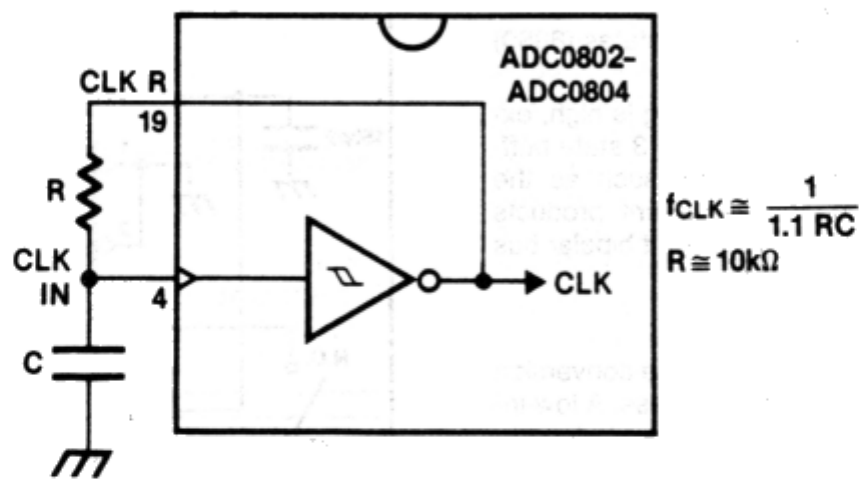
Heavy capacitive or DC loading of the CLocK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

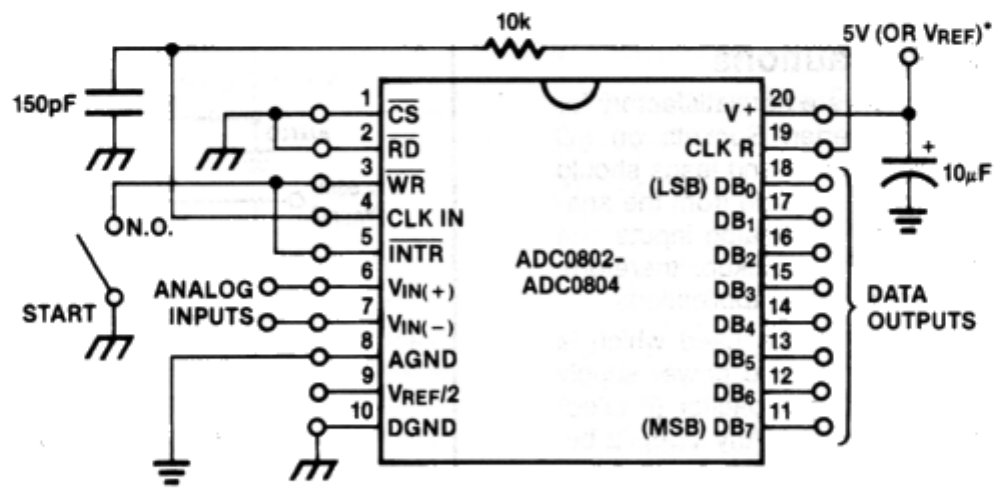
Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 12 for details.



0334-26

Figure 11: Self-Clocking the A/D



0334-27

Figure 12: Free-Running Connection

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

INTERSIL

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in 3-state (high-impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see **Typical Performance Characteristics).**

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be 3-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V^+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V^+ pin, and values of 1μF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V^+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see **Zero Error** for measurement). Further information can be found in A018.

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 13.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V^+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090V (5.120 – 1½ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

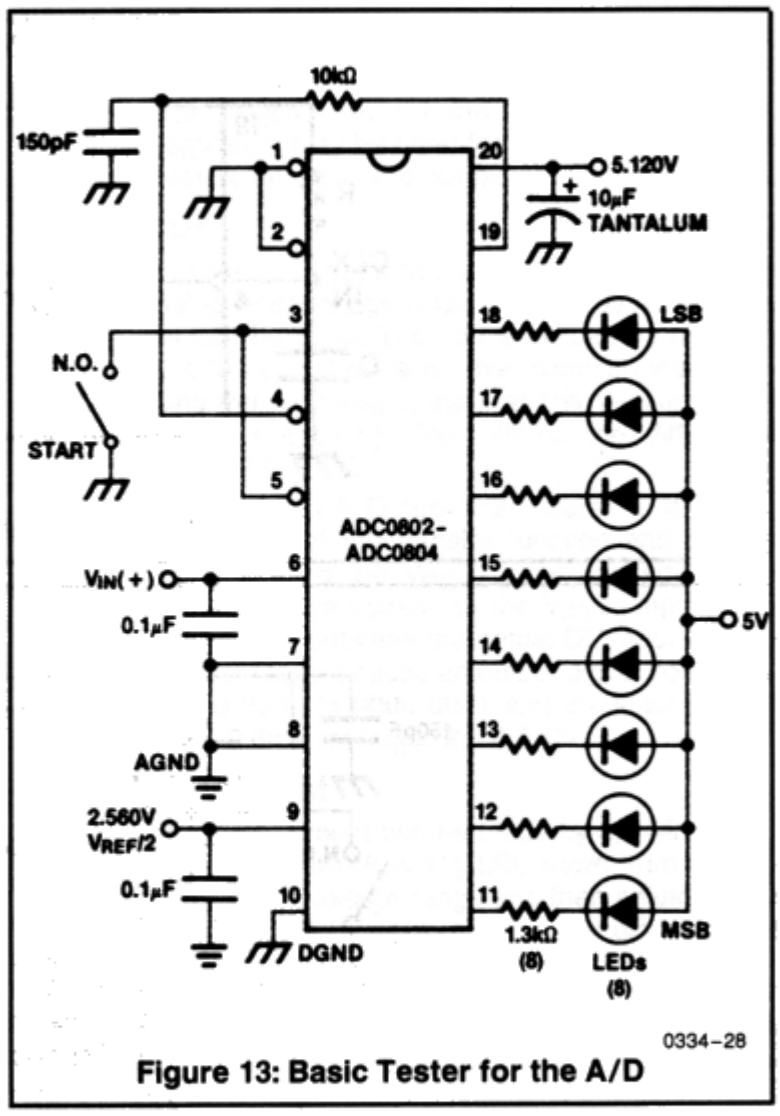


Figure 13: Basic Tester for the A/D

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full-scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)V.$$

NOTE: All typical values have been characterized but are not tested.

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.64V.$$

Figures 14 and 15 show more sophisticated test circuits.

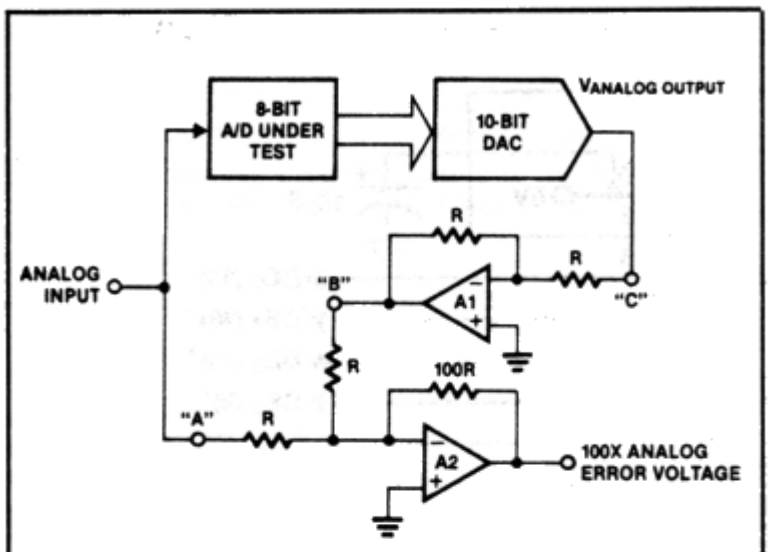


Figure 14: A/D Tester with Analog Error Output. This circuit can be used to generate "error plots" of Figure 6.

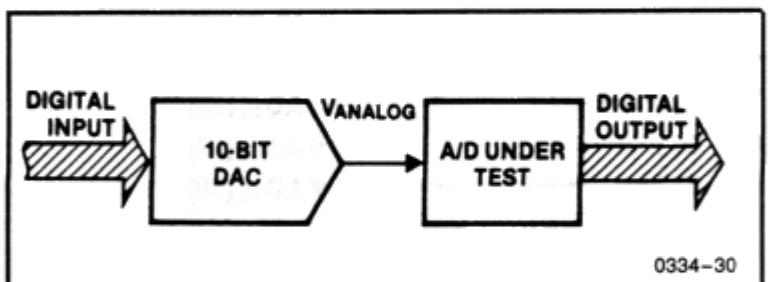


Figure 15: Basic "Digital" A/D Tester

APPLICATIONS

Interfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See A020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 16.

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 17. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 17 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO}$/M for an I/O-mapped connection.

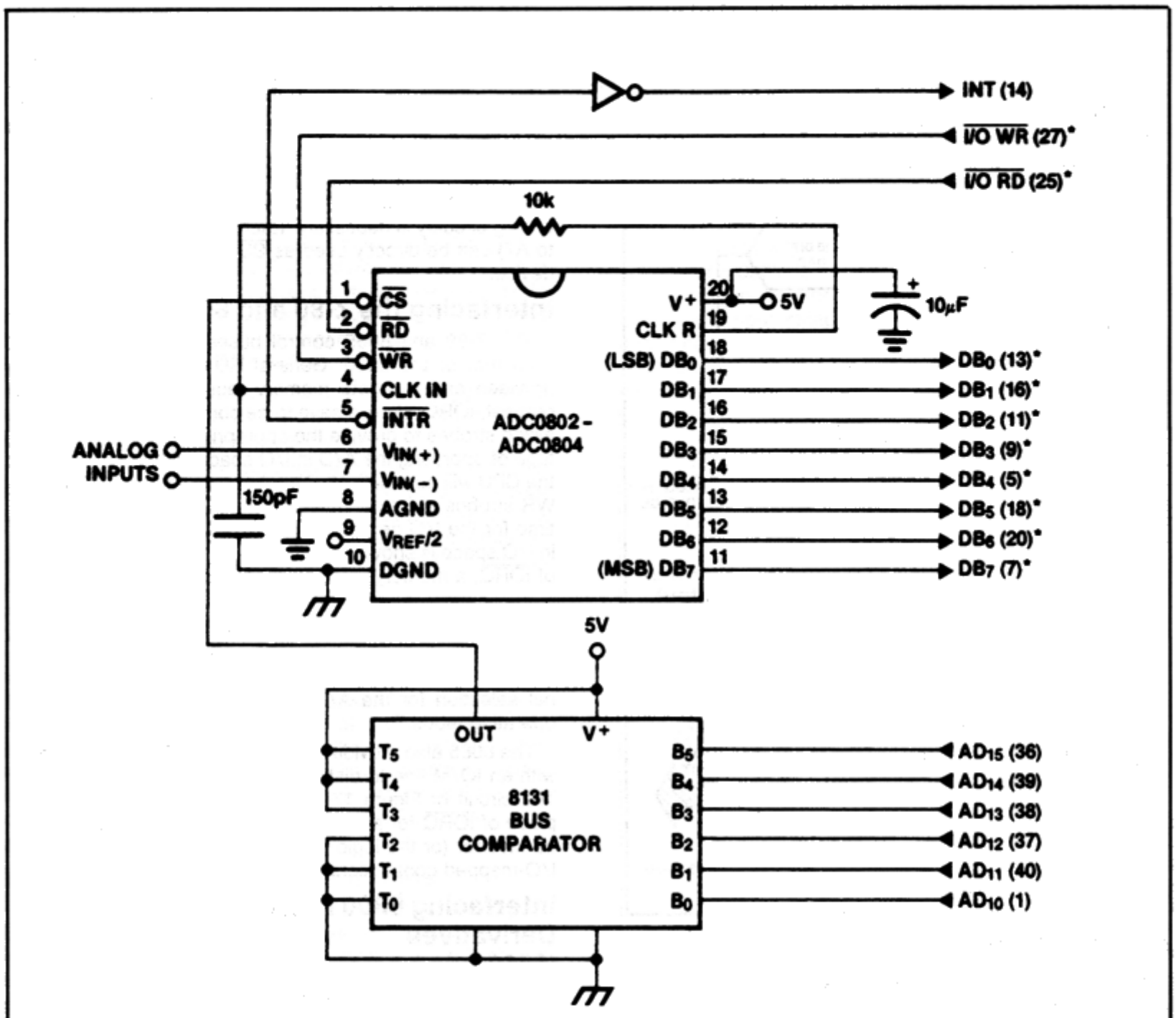
Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 16 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 19 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804



Note: Pin numbers for 8228 system controller: others are 8080A

Figure 16: ADC0802 to 8080A CPU Interface

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

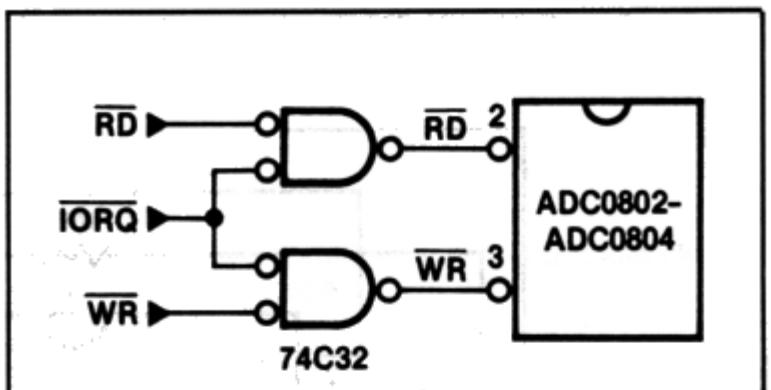
A016 "Selecting A/D Converters," by Dave Fullagar.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.

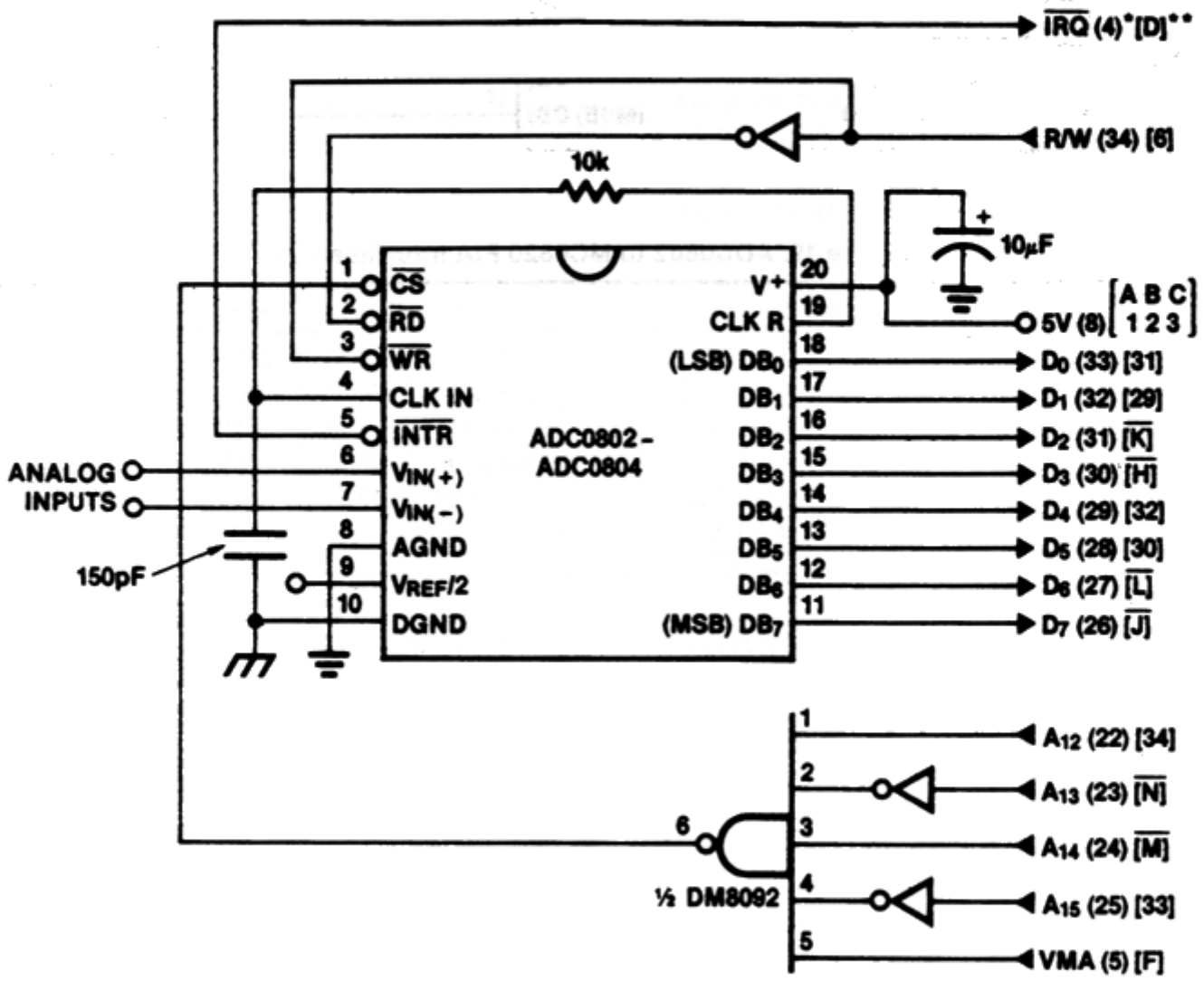
A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.



0334-32

Figure 17: Mapping the A/D as an I/O device for use with the Z-80 CPU



0334-33

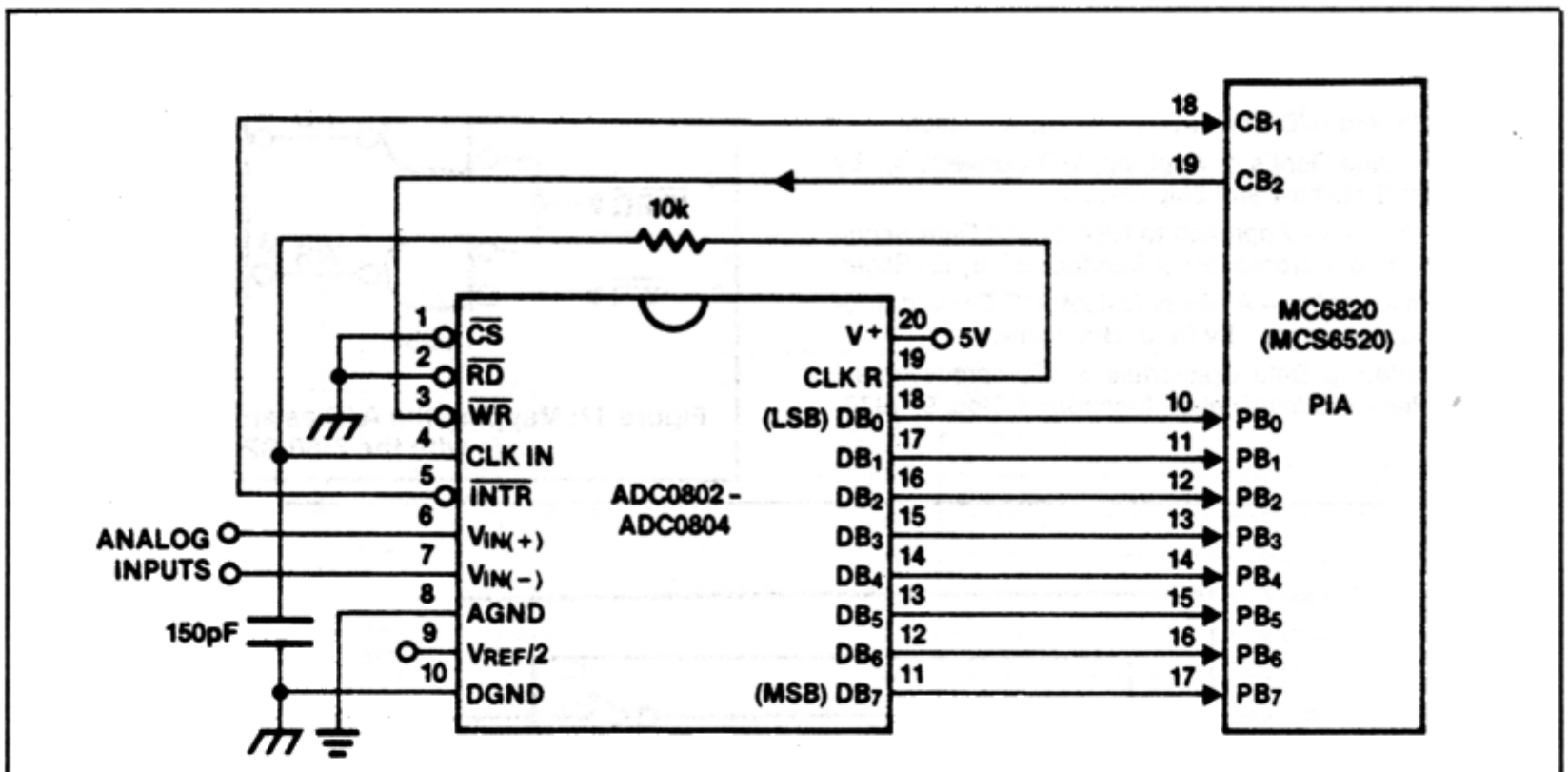
***Note 1:** Numbers in parentheses refer to MC6800 CPU pinout.

****Note 2:** Numbers or letters in brackets refer to standard MC6800 system common bus code.

Figure 18: ADC0802 to MC6800 CPU Interface

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804



0334-34

Figure 19: ADC0802 to MC6820 PIA Interface

NOTE: All typical values have been characterized but are not tested.